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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/770,711	02/02/2004	Paul J. Steffan	H0897	2278

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EXAMINER	
DIMYAN, MAGID Y	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/770,711	STEFFAN, PAUL J.	
	Examiner	Art Unit	
	Magid Y. Dimyan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This pertains to Application No. 10/770711, filed 02 February 2004. Claims 1 – 20 are pending in this Application.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a) because they fail to show the steps represented by blocks 402 – 408, as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 – 20 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,901,564 B2 to Stine et al. (hereinafter, "Stine").

5. Pursuant to claims 1 and 11, Stine discloses a method (claim 1) and a system (claim 11 – see also col. 1, ll. 13 – 15) for facilitating wafer lot disposition (see col. 2, ll. 43 – 55) comprising: a) providing detailed descriptive information of the semiconductor wafer layout (see Figs. 1 and 2, block 12; col. 1, ll. 17 – 59; col.4, ll. 51 – 59); (b) generating data concerning at least one defect in the semiconductor wafers at an intermediate stage (see col. 4, ll. 41 – 59; col. 5, ll. 40 – 51); (c) generating at least one layer model from the information and data to disclose the effects of the defect upon at least one later layer of the semiconductor layer (see col. 3, line 65 – col. 4, line 40, which cite how the model generated for a process level can be used to predict yields for subsequent wafer levels); and (d) utilizing the layer model to determine the subsequent disposition of the wafer lot (see again Figs. 1 and 2; col. 3, line 65 – col. 4, line 40 which cite these elements). Stine thus clearly teaches all the claimed limitations.

6. As to claim 2 and 3, see col. 4, ll. 18 – 40, which recite the claimed limitations pertaining to generating and utilizing the layer model and disclosing the components located above a defect in a wafer.

7. Regarding claim 4, see col. 16, line 60 – col. 21 line 26, which describe in detail the likely cause of defects in subsequent layers (open/short circuits, via problems, etc) as claimed.

8. As per claim 5, see col. 4, ll. 51 – 59, which cites a GDS2 layout on a tape or disc (i.e., an electronic description of the wafer layout) for every layer in the semiconductor wafers' fabrication process, as claimed.

9. Referring to claims 6 and 16, Stine discloses a method (claim 6) and a system (claim 16 – see also col. 1, ll. 13 – 15) for facilitating wafer lot disposition (see col. 2, ll. 43 – 55) comprising: a) providing detailed descriptive information of the semiconductor wafer layout (see Figs. 1 and 2, block 12; col. 1, ll. 17 – 59; col.4, ll. 51 – 59); (b) generating and extracting data concerning at least one defect in the semiconductor wafers at an intermediate stage (see Figs. 1 and 2, block 18; col. 4, ll. 41 – 59; col. 5, ll. 40 – 51); (c) generating at least one layer model from the information and data to disclose the future effects of the defects upon later layers at subsequent stages of the fabrication process (see col. 3, line 65 – col. 4, line 40; col. 5, ll. 1 - 39, which cite how the model generated and extracted for a process level can be used to predict yields for subsequent wafer levels); and (d) utilizing the layer model to determine the subsequent disposition of the wafer lot (see again Figs. 1 and 2; col. 3, line 65 – col. 4, line 40 which cite these elements). Stine thus clearly teaches all the claimed limitations.

10. Claims 7, 12 and 17 contain the same limitations as claim 2, and therefore the same rejection applies.

11. Claims 8, 13 and 18 contain the same limitations as claim 3, and therefore the same rejection applies.

12. Claims 9, 14 and 19 contain the same limitations as claim 4, and therefore the same rejection applies.

13. Claims 10, 15 and 20 contain the same limitations as claim 5, and therefore the same rejection applies.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 3,751,647 to Maeder et al. discloses yield modeling for an IC manufacturing process that utilizes the number of defects for each chip, rather than average defect density, in the prediction model.

U.S. Patent No. 6,980,873 B2 to Shen provides a system and method for detecting a fault and identifying a remedy for the fault in real-time in a semiconductor product manufacturing facility.

Pub. No. US 2002/0165636 A1 to Hasan teaches systems and methodologies for generating setup information for using measuring process parameters associated with semiconductor devices.

U.S. Patent No. 6,912,439 B2 cites systems and methods of modeling a best-guess semiconductor process flow for fabricating a desired semiconductor device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y. Dimyan whose telephone number is (571) 272-1889. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Magid Y Dimyan
Examiner
Art Unit 2825

myd
20 March 2006

STACY A. WHITMORE
PRIMARY EXAMINER